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**XEDA**

**Jan 21, 2021**



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**Xeda** /*zid*/ is a cross-platform, cross-EDA, cross-target automated synthesis and simulation platform. It helps hardware developers to verify, evaluate, and deploy their RTL designs using multiple commercial and open-source electronic design automation flows.



# CHAPTER 1

## Quickstart

To get started with xeda, first create a `design.json` file for your design. This file contains metadata, list of source files, and flow settings regarding your design. Below is an example `design.json` which can be adapted to any design.

```
{
  "design": {
    "name": "mydesign",
    "description": "This really cool design",
    "author": ["Dr. Seuss", "[Xena] (https://en.wikipedia.org/wiki/Xena)", "[Kamya↵
    ↵Mohajerani] (mailto:kammoh@gmail.com)"],
    "url": "https://github.com/KeccakTeam/Xoodoo.git",
    "sources": [
      "src_rtl/v1/s1.vhd",
      "src_rtl/v1/s2.vhd",
      {
        "file": "src_tb/tb_s.vhd",
        "sim_only": true
      }
    ],
    "vhdl_std": "02",
    "vhdl_synopsys": true,
    "top": "TOP",
    "clock_port": "clk",
    "tb_top": "TB_TOP",
    "tb_generics": {
      "STRING_GENERIC": "hello",
      "FILENAME_STRING_GENERIC": {
        "file": "../data.txt"
      },
      "INT_GENERIC": 123
    },
    "generics": {}
  },
  "flows": {
```

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```
"diamond": {
  "fpga_part": "LFE5U-25F-6BG381C",
  "clock_period": 11.061946902654867,
  "synthesis_engine": "synplify",
  "strategy": "Timing"
},
"vivado": {
  "fpga_part": "xc7a12tcsq325-3",
  "clock_period": 4.369,
  "strategy": "Timing",
  "optimize_power": "False",
  "sim_run": "all"
}
}
```

After the `design.json` file has been created for your design, you can now use `xeda` to generate simulation, synthesis and implementation results for your design using the supported tool of your choice.

For example, if we want to simulate the above design with GHDL, we would run

```
$ xeda run ghdl_sim
```

If our `design.json` file is renamed or not in the directory that `xeda` is called in, we can explicitly specify the path of the file with the `--design-json` argument

```
$ xeda run --design-json xeda_configs/design_1.json ghdl_sim
```

If we are satisfied with the results of the simulation, we can have `xeda` synthesis and implement our design. For example, with Xilinx Vivado:

```
$ xeda run vivado_synth
```

That's it! That's all `xeda` requires to simulate, synthesis, and implement an HDL design.

As always, you can run `xeda --help` or `xeda run --help` for the full list of arguments



### 2.1 Reports Directory

`reports_subdir_name` is the name of the default reports subdirectory within a flow's `run_dir`. All the tools in a flow save their `_report_` files inside this directory. The files in this directory will be parsed during execution of a flow's `parse_report()`.



## CHAPTER 3

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